underlining for added matter. No new matter has been added to the Substitute Specification.

In the Drawings:

Please replace previously submitted formal Figures 1A, 1B, and 2 with the corrected marked-up informal versions thereof submitted herewith, wherein revisions to Figures 1A, 1B, and 2 have been indicated in red ink.

In the Claims:

Please cancel, without prejudice, originally submitted Claims 1-3.

Please add newly presented Claims 4-9 as follows:

4. A self-locking memory circuit for a tri state data bus having multiple bit lines, said self-locking memory circuit comprising:

a non-clocked, non-inverting amplifier chip for connection to one of said bit lines; and

a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip;

said self-locking memory circuit having upper and lower voltage thresholds that cause said self-locking memory circuit to change states when a level of voltage applied to said self-locking memory circuit passes through one of said thresholds.

5. A programmable system comprising:

a central processing unit;

a Digital Signal Processor for transceiving discrete electrical inputs; and

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a tri state data bus electrically connecting said Digital Signal Processor to said central processing unit;

said Digital Signal Processor and said central processing unit having different clock rates for accessing said tri state data bus; and

self-locking data bus circuits connected to respective bit lines of said tri state data bus for maintaining said respective bit lines of said tri state data bus in their last driven state during said access of said tri state data bus by Digital Signal Processor and said central processing unit at said different rates.

6. The programmable system according to Claim 5, wherein said system further includes:

a Complex programmable Logic Device for transceiving discrete electrical signals;

a tri state data bus electrically interconnecting said central processing unit, said Digital Signal Processor, and said Complex Programmable Logic Device;

said Digital Signal Processor and said Complex Programmable Logic Device having clock rates for accessing said tri state data bus that are different from a clock rate at which said central processing unit accesses said tri state data bus; and

self-locking data bus circuits connected to respective bit lines of said tri state data bus for maintaining said respective bit lines of said tri state data bus in their last driven state during said access of said tri state data bus by Digital Signal Processor, said Complex Programmable Logic Device, and said central processing unit at said different rates.

7. The programmable system according to Claim 5, wherein each of said self-locking data bus circuits includes:

a non-clocked, non-inverting amplifier chip for connection to one of said bit lines; and

a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip;

said self-locking memory circuit having upper and lower voltage thresholds that cause said self-locking memory circuit to change states when a level of voltage applied to said self-locking memory circuit passes through one of said thresholds.

8. A programmable system comprising:

a central processing unit;

a Complex Programmable Logic Device for transceiving discrete electrical inputs; and

a tri state data bus electrically connecting said Digital Signal Processor to said central processing unit;

said Complex Programmable Logic Device and said central processing unit having different clock rates for accessing said tri state data bus; and

self-locking data bus circuits connected to respective bit lines of said tri state data bus for maintaining said respective bit lines of said tri state data bus in their last driven state during said access of said tri state data bus by Complex Programmable Logic Device and said central processing unit at said different rates.

9. The programmable system according to Claim 8, wherein each of said self-locking data bus circuits includes:

a non-clocked, non-inverting amplifier chip for connection to one of said bit lines; and

a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip;